Chasing a Latent CDM ESD Failure by Unconventional FA Methodology

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Abstract – A hard-to-detect functional CDM ESD failure caused by an obscure charge trapping phenomenon on an advanced CMOS IC is described while no physical damage was evident. Advancing failure analysis method by localized thermal LASER annealing and applying analytical ESD test plan led to successful localization of the root cause.

I. Introduction

Continuous scaling of CMOS technologies and bid to integrate more and more functionality on a single chip has made IC design more complex and challenging. Furthermore, for ESD qualification, the IC has to pass all the performance tests within specification limits after applying the ESD stress. The latest CMOS technologies comprise devices with ultra thin gate dielectrics which are extremely sensitive to overvoltage [1-5]. ESD stress can lead to failures seen as hard damage to devices or inter-connects, increased leakage or loss of functionality. ESD damage can be catastrophic or latent [5-7] in nature. ESD failures of catastrophic nature are well understood and are comparatively simple to find in Failure Analysis (FA). On the other hand, latent or soft failures are often not easily visualized. The exact mechanisms of soft fails are subjects for further research.

Failure Analysis (FA) of ESD failures is a very important part of the product design cycle [8, 9]. FA helps to provide deep insight into root cause of failures and developing new ESD solutions or workarounds. Typically the FA workflow involves the following steps:

a) Reproduction of ESD fails by electrical tests in the lab,

b) Localization of the ESD fails,

c) Physical inspection to check the damage.

The localization of latent failures is a very complex task as many of the traditional FA methods usually fail to provide any significant information on the location of the failing devices.

In this paper we discuss the failure analysis investigations done on an IC and the development of a novel method which helps in localizing ESD failures – in this case due to charge trapping. The background of the ESD issue, the conventional FA results and the analytical testing are discussed in section II. In section III & IV, we describe the new FA localization method and the experimental setup respectively. The section V demonstrates the results and section VI concludes the paper.

II. Background

During the ESD qualification of an IC fabricated in an advance technology node, failures were seen after applying 500V CDM stress where 2 of 3 ICs failed.

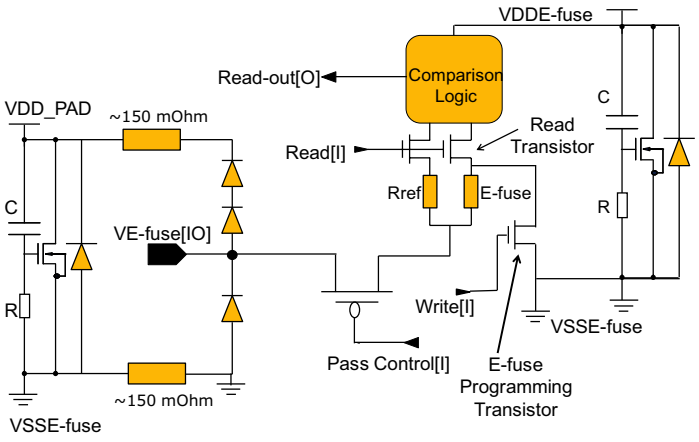

Figure 1: E-fuse sensing logic and the ESD protection network.

The fails were seen in functional tests where the ICs had discrepancies in the Electrical-fuse (E-fuse) read

out and were unable to enter the "Deep Sleep Mode." Similar failures were also seen at a higher stress of 750V CDM, for which all 3 of 3 ICs failed. The E-fuse failure was statistical and not all of the E-fuses on the chip were failing. There was no correlation between the failing fuses on the various failed ICs. The connectivity of the E-fuse block to the VE-fuse programming pin and the ESD protection network is shown in Fig.1. The resistance of the VDD_PAD & VSSE-fuse bus in the E-fuse pad to the power clamp between VDD_PAD and VSSE-fuse was 150 mOhm. The VDDE-fuse/VSSE-fuse core domain is a very large domain with multiple RC triggered clamps. The VE-Fuse pin is protected with diodes to the VDD_PAD supply and VSSE-Fuse. The primary current path for CDM current when substrate is charged positive and VE-Fuse pin is grounded is from the VSSE-Fuse through the diode connected to the VE-Fuse [IO] pin. When the substrate is negatively charged and the VE-Fuse pin is grounded, the current flows from the VE-Fuse pin via pair of diodes and the RC triggered clamp to the substrate. The applied ESD protection concept was already successfully qualified for 500V CDM stress level (I_{CDM}=4A) on other ICs.

E-fuses are used for chip identification, redundancy and for setting trimming values. The E-fuses work on the principle of resistance change through electro-migration. During programming of the E-fuse, current flows for certain time duration from the VE-fuse [IO] pin - via the PMOS pass transistor, through the fuse link which is a polysilicon resistor and the E-fuse programming transistor, which causes the E-fuse resistance to change significantly due to electro-migration. During the E-fuse readout, the E-fuse resistance is compared with a reference resistor Rref. A "0" or logic "low" at Read-out [O] indicates that the E-fuse is intact or "unblown", whereas a "1" or logic "high" indicates that the E-fuse is "blown". The pins Read [I], Write [I], Pass Control [I] and Read-out [O] are connected to internal core circuits in the same power domain. There is also a possibility for comparison of the E-fuse resistance with a higher reference resistance to check the margin of the fusing. The PMOS pass transistor is on during E-fuse programming only and is off during the normal operation. In case of the E-fuse failures some fuses which were "unblown" before ESD stress were read out as blown after the ESD stress. When the comparison of the failed E-fuses was done with the higher reference resistance, all these E-fuses exhibited the correct logic readout. The failing ICs were sent for physical failure analysis along with some reference ICs to find out the root cause of the fails. As first step for the FA, the E-fuse readout patterns were installed on the FA test system. The E-fuse readout at the FA lab confirmed the failures as reported after the qualification tests. The readout vectors exhibited an unexpected logic "high" instead of an expected logic "low" which corresponds to "blown" E-fuses (Fig. 2).

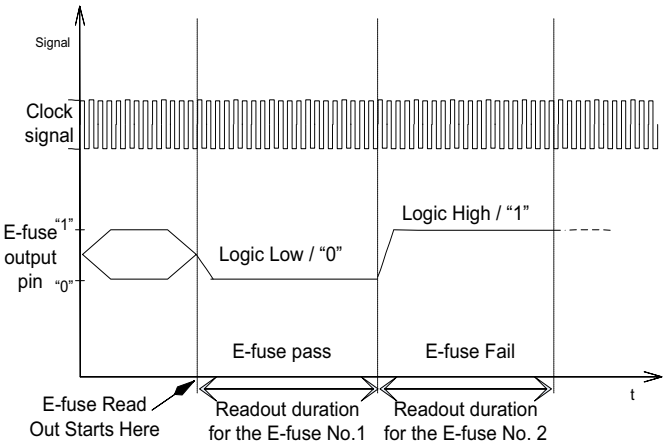

Figure 2: Readout of the test system shows failing E-fuses after CDM ESD stress.

For the localization step, photon emission microscopy (EMMI) was performed with the application of the same electrical patterns on both, failing and reference ICs. The EMMI localization step (Fig. 3) did not reveal any significant differences between the failing and the reference ICs.

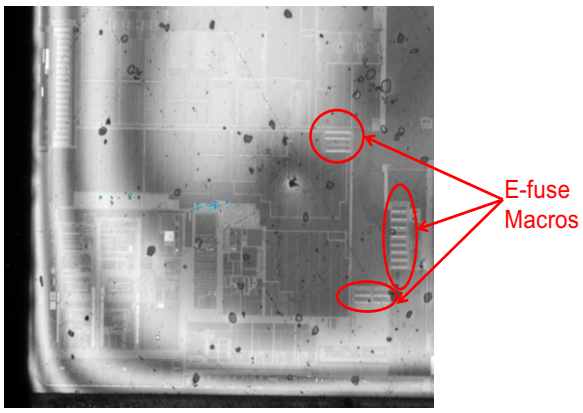

Figure 3: The EMMI image of the failing IC shows no spots which are related to E-fuse readout.

It was suspected that the E-fuse link resistance was significantly altered due to ESD stress based on the observation from comparison with higher reference resistance. A layer lift-off was done down to the fuse link layer and Scanning Electron Microscope (SEM) inspection was performed to observe potential damage to the fuse link (Fig. 4). After the inspection it was

confirmed that the reported failing fuse link did not have any visible damage.

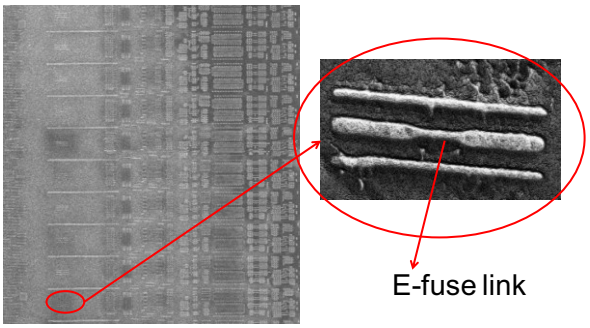

Figure 4: The SEM view of the reported failing E-fuse after lift-off. No damage to the fuse link is seen.

An SEM inspection of the transistors of the E-fuse sensing circuit was also done to check if there was any damage to the sensing circuitry which would have led to an incorrect read out. However, the devices of the sensing circuit also had no visible damage. To rule out damage to the silicide layer as a part of the suspected polysilicon failed fuse link, a Transmission Electron Microscope (TEM) inspection was done on another sample with similar failures at 750V CDM. Even for a higher ESD level there was no visible damage to the silicide layer (Fig. 5, 6).

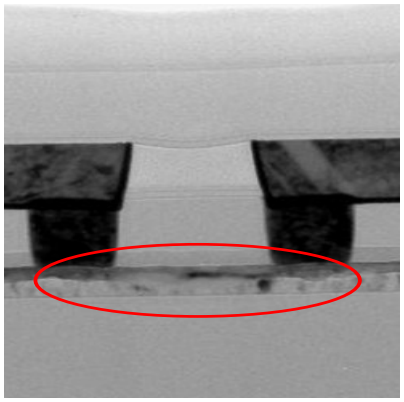

Figure 5: TEM image of the cross-section of the E-fuse link.

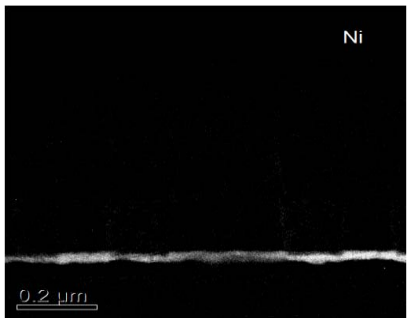

Figure 6: Energy filtered TEM image shows silicide layer is intact. Scan for nickel from the nickel silicide.

Additionally, preparation down to contact level was done for resistance measurement and the resistances of the fuse links were measured using the four point contact method for both reported failing and passing E-fuses. However, the resistance of the reported failing E-fuse link was found within the limit of an unblown E-fuse (Fig 7).

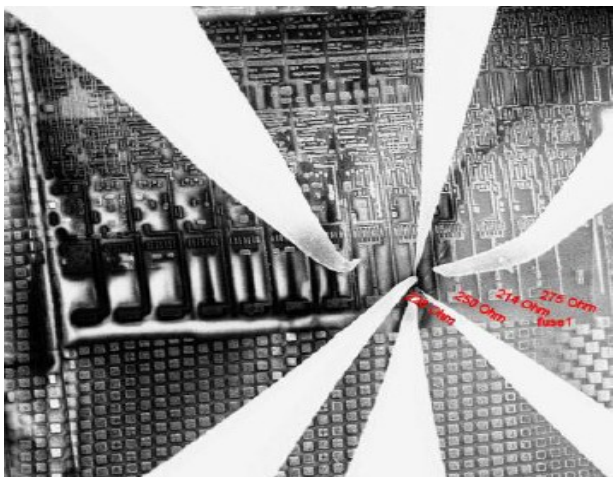

Figure 7: Resistance measurement of the E-fuse links using four point contact method.

Up to now with the conventional FA methods, no localization of the failure was possible. The conventional methods did successfully rule out any damage to the E-fuse link which was the "prime suspect" in this case. Latent failure due to charge trapping was suspected as the reason of failure. Therefore, a thermal annealing treatment for de-trapping was performed. In this experiment the IC was baked in an oven at a constant temperature of 120 deg. C for 24 hrs. After the thermal annealing treatment the IC was remeasured. The e-fuse readouts were back to normal i.e. all the failing E-fuses had the pre-ESD stress values.

The focus was now shifted to produce a hard failure by overstressing the IC and perform an FA afterwards to see if we could locate the failing device. Some ICs were stressed at 750V CDM with a high number of stress pulses per pin instead of the standard JEDEC procedure. The overstress experiment did not yield any information regarding the failing devices as overstress caused additional multiple failures which were not relevant to the analysis and there was again no hard damage seen for the relevant fails. Further CDM tests were conducted to find out which polarity of stress and stress on which pin caused the failures. The following table sums up the list of tests performed.

Table 1: Test plan performed to check the polarity of stress causing failure and identify the weak pin

Test No.	Stress Level (V)	Stress Polarity	Pin(s) stressed	Result
1	750	Positive	All pins	Pass
2	750	Negative	All pins	Fail
3	750	Negative	All except VDDE-fuse pin	Fail
4	750	Negative	Only VDDE-fuse pin	Pass
5	750	Negative	All except VSSE-fuse pin	Fail
6	750	Negative	Only VSSE-fuse pin	Pass
7	750	Negative	All except VE-fuse pin	Pass
8	750	Negative	Only VE-fuse pin	Fail

The latest series of CDM tests confirmed that the weakness was only for the negative polarity. From the test results it became clear that the weakness was related to the VE-fuse pin which is used for programming the E-fuses. From these tests and the FA results, the suspect was now the E-fuse logic connected to the VE-fuse IO pin. Every E-fuse has a separate sensing logic and we suspected that the reported failing E-fuses might exhibit malfunctioning of the E-fuse sensing logic. The E-fuse sensing logic consisted of a large number of transistors, where degradation on several of them could cause the observed electrical failure signature. This lead to a further complicated situation where depending on the exact location of the failing device(s) different correction measures had to be applied. The localization of the degraded device(s) was therefore important for decision on the ESD protection measures.

III. New FA Methodology: Local Annealing

As we found out earlier, the ESD failures were recoverable by thermal annealing of the IC. So, if it is possible to do thermal annealing at a local level or heating of the individual device, then we could also localize the failing devices by identifying if a failure is gone by heating a particular device. In this case, the suspected devices were from the failing E-fuse sensing logic. The challenge for the above approach was to find a method to heat devices locally and very precisely. The location of the failing E-fuse cells within the large E-fuse banks was known and this reduced the amount of area to be considered by the local heating method. We decided to use a laser source for heating devices locally. Thermal Laser Stimulation (TLS) has been used in the past to heat interconnects and devices [10, 11] but not in case of fails due to charge trapping. For precise localization of failing devices a clear "recovery" of the proper electrical fuse readout ("unblown fuse") is desired. In the following section we describe the setup for the local annealing experiment.

IV. Experimental Setup

1. Setup & Preparation

The IC was prepared from backside down to a thickness of ca. 100um. The setup for local annealing is shown in Fig.8. The failing IC was placed on the test board which in turn was mounted in a system housing the laser source, the DUT with test board, a scanning microscope and the control system for the microscope. The laser scanning was done with a laser scanning microscope.

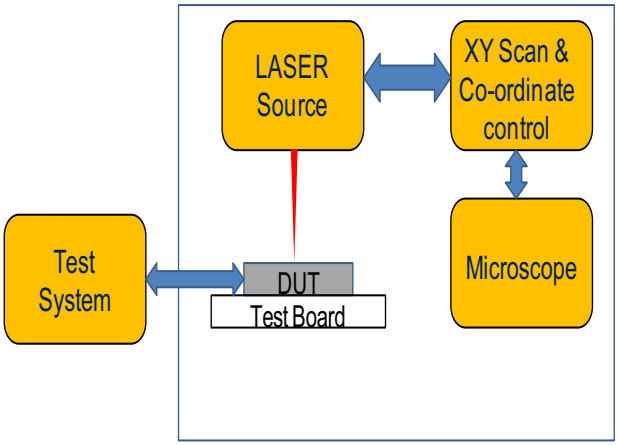

Figure 8: Experimental setup to perform local thermal annealing.

The wavelength of the laser used was 1.3um. The reflected radiation can be used as input for the imaging system such that an optical image of the IC is obtained. With a 50x/100x lens and 2x zoom factor, a line scan was performed and in parallel the test system is used to read out the E-fuse output vectors. The maximum power available for the laser is 400 mW. The beam diameter of the laser is approximately 1.5um. Typical local temperature rise achieved with the above setup is about 1 °C/mW of laser power as reported by Cole [12].

2. Procedure

The device was scanned with the laser beam which induces a local heating at the devices underneath. The

test system provides the electrical test pattern and also reads out the E-fuse vectors at the output pin continuously and simultaneously as the laser scans the DUT. The location of the beam, where the E-fuse vector changes from fail to pass, is correlated with the location of the failing or degraded devices. The duration of the laser line scan is longer as compared to the readout duration of the complete E-fuse bank. This makes sure that the laser scan can be stopped as soon as there is a change in the E-fuse readout. An area scan with the laser beam is additionally enabled in the setup.

V. Results & Discussion

The initial readout shows failures at a large number of E-fuses from the E-fuse banks (Fig. 2). Different locations in the E-fuse banks were scanned with the laser. When the scan was done along a particular line, along which the transistors connected to the E-fuse link are located (Fig. 9), recovery from the electrical failures was noticed. From this line scan the y coordinate of the failing device was identified.

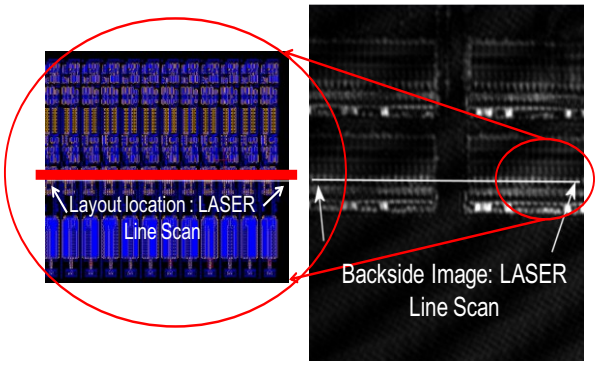

Figure 9: Location of the laser horizontal line scan along which the failures were reduced.

An additional laser area scan from the vertical direction was performed to locate the failing device with better precision. The laser starts scanning the area and moves in the vertical direction. As soon as the failing transistor of the E-fuse logic is annealed and the error cycles reduce, the scan is stopped. From the vertical scan the x coordinate of the device was identified. The area where the laser scanning was done is marked in red (Fig. 10) and the location where the E-fuses readout was recovered to the original value is marked by a green dot. The relative location of laser line scan from previous experiment is depicted by a white dashed line. With laser power at 50% of its maximum value, it was detected that the value of the E-fuse readouts returned to the ones from pre-ESD stress values. This recovery is of permanent nature and remains even when the laser stimulation is removed. The readout of E-fuses after a line scan of 2 large E-fuse banks for the same NMOS transistors reduced errors significantly.

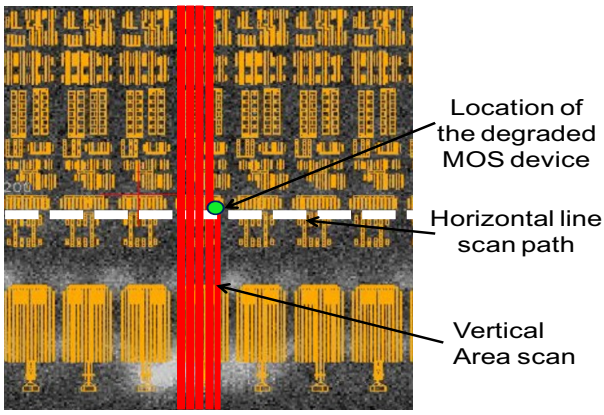

Figure 10: Overlay of the laser area scan image in vertical direction with layout.

This method, thus, successfully localized the failing devices which could not be localized with the conventional FA methods (Fig. 11).

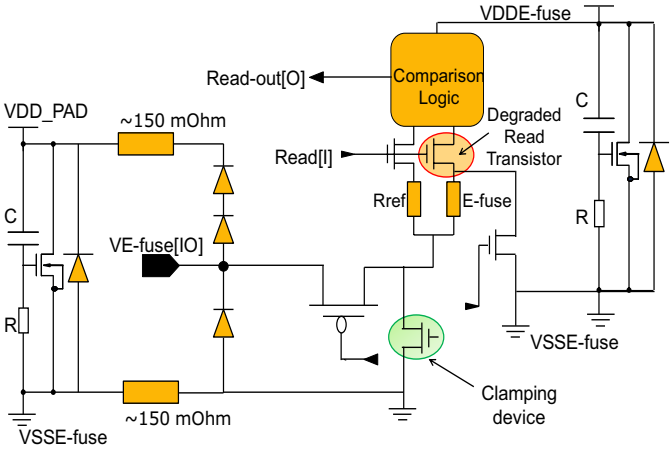

Figure 11: Location of the degraded device and the implemented ESD fix.

The CDM related failure mechanism could be explained by coupling of a voltage transient through the large PMOS pass transistor to the E-fuse sensing circuits, which led to the degradation of a transistor remote from the stressed pad. During the CDM stress with a negative substrate bias (-500V), the NMOS encircled in red in Fig.11 experiences a strong positive drain-bulk voltage and because of the floating gate – a moderate positive gate-bulk voltage stress, while the source is assumed to be at substrate potential. The high electric field at the drain-side leads to avalanche-generated electrons having high kinetic energy. These “hot” electrons get injected into the gate dielectric. The consequence is a positive shift of

the NMOS threshold voltage (Vt) because the negative charge in the dielectric has to be compensated by a higher positive gate bias. This is in accordance with the observed critical CDM ESD stress polarity (negative substrate) and a simulated threshold shift of 140mV which can mimic the degradation in circuit simulation. By modeling an increase in Vt in SPICE simulations, the observed circuit's malfunction could be reproduced. Note that the E-fuse programming transistor is also susceptible to hot carrier induced charge trapping, but Vt shifts in this device do not affect circuit functionality as it is off during normal operation. To fix this issue a local active ESD clamping device has been added to the internal node after the PMOS pass transistor as highlighted in green in Fig. 11. The device clamps the internal node during the CDM event thereby reducing the voltage at this node and protecting the devices connected to this node. ICs with the updated ESD concept using the above mentioned fix pass 500V CDM, I_{CDM}= 4.8A.

A brief summary of the applied test and FA flow and the result from each step is indicated in the Fig. 12.

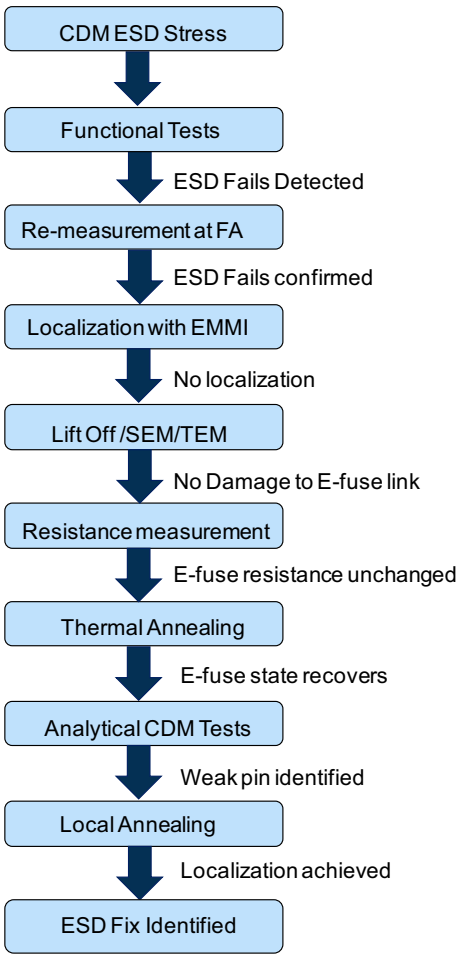

Figure 12: Applied Test and FA methods and their outcomes.

We observed the annealing behavior and E-fuse recovery on all ICs which were investigated using the local annealing method. The E-Fuse recovery was also seen on an IC to which ten 750V CDM pulses per pin were applied and thermal annealing at 120 deg C for 24 hours did not lead to recovery of E-fuses. The recovery of the E-fuses after applying different methods and the percentage of E-fuses recovered is summarized in Table 2.

Table 2: Summary of FA methods used and recovery of E-fuses

Part. No.	CDM Stress Level (V)	No. of Failing E-fuses	Method Applied	Percentage of E-fuses recovered
1	500	0	NA	NA
2	500	8	Lift-off and SEM	NA
3	500	60	TEM and Resistance measurement	NA
4	750	30	Thermal Anneal (120°C for 24Hrs.)	100%
5	750	54	Thermal Anneal (120°C for 24Hrs.)	100%
6	750	52	Local Anneal (~200mW)	~96%
7	750 (3x)	44	Local Anneal (~200mW)	~91%
8	750 (10x)	55	Thermal Anneal (120°C for 24Hrs.) / Local anneal (200mW)	0% / ~90%

As a final experiment, a laser scan on a selected area of the failing E-fuses with the IC in power-off state was performed. This experiment was performed to clarify whether the fuse recovery was only due to the

laser stimulation or if the recovery was a combined effect of laser stimulation and the biasing conditions. An E-fuse vector read out was performed both before and after the laser scan. The readout of the E-fuse vectors after the laser scan in IC power-off confirmed that 7 failing E-fuses in the scanned area were recovered. Another laser scan of the same area was performed with the IC powered on. No additional recovery of E-fuses was observed. This indicates that the local annealing is only dependent on the laser stimulation and is independent of the biasing conditions.

The independence of the method on biasing conditions is one advantage of this localization method for the observed failure mode. Another important feature of the local annealing method is that it is non-destructive. The laser stimulation process does not introduce the danger of further mechanical or thermal damage to the sample. Also the sample preparation for this method is similar to the EMMI back side localization and does not involve heating steps, which would cause recovery of the device before the localization step is performed.

The limitation of this approach is that it is only applicable to fails due to charge trapping and requires significant set up time. There is also a limitation of the accuracy of localization in the order of the wavelength of the laser. This can potentially be relaxed by incremental stepping of the scanning beam.

VI. Conclusion

In this study, a combination of conventional FA methods, analytical stress testing and a novel application of laser scanning to locally anneal small IC regions allowed the localization of a device which was degraded by CDM stress. The failing device was identified as a single transistor which is subject to gate oxide charge trapping degradation during CDM stress, failing in a statistical manner. This novel localization method provides a unique way to debug a critical failure class widely seen during CDM stress of modern ICs.

Acknowledgements

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